Amendments to the Claims

Please amend the claims as follows:

1-2. (Canceled).

3. (Currently Amended) The memory circuit according to claim [[2]] 12, wherein when the redundant replacement unit having the failed portion is replaced with the redundant memory cell array, a pre-charge switch corresponding to the redundant memory cell array conducts.

4. (Currently Amended) The memory circuit according to claim [[1]] 12, wherein the regular memory cell array and the redundant memory cell array have a plurality of memory cells and a plurality of bit lines connected to the plurality of memory cells, the plurality of bit lines being pre-charged by the pre-charge circuit.

5. (Original) The memory circuit according to claim 4, wherein

the memory cell is a static memory cell.

6. (Withdrawn) A memory circuit comprising:

a regular memory cell array;

a redundant memory cell array which enables to replace a failed portion in the regular memory cell array; and

a redundant replacement memory for storing data on the failed portion in the regular memory cell array, wherein

the redundant replacement memory includes a redundant cell holding failed portion data, and a redundant latch circuit for latching the failed portion data held by the redundant cell,

depending on the data latched by the redundant latch circuit, the failed portion is replaced with the redundant memory cell array, and

the redundant latch circuit latches test data supplied from an external terminal during testing, for temporary replacement with the redundant memory cell array.

7. (Withdrawn) The memory circuit according to claim 6, wherein

during the testing, the supply of the failed portion data held by the redundant cell to the redundant latch circuit is prohibited.

8. (Withdrawn) The memory circuit according to claim 6, wherein

the redundant replacement memory includes a first switch interposed between the redundant cell and the redundant latch circuit, and a second switch interposed between the external terminal and the redundant latch circuit, and wherein

during regular operation, control is provided such that the first switch is conducting and the second switch is non-conducting, whereas during the testing, control is provided such that the first switch is non-conducting and the second switch is conducting.

9. (Withdrawn) The memory circuit according to claim 8, wherein

during the testing, control is provided such that the second switch temporarily conducts and thereafter goes non-conducting.

10. (Withdrawn) The memory circuit according to claim 6, wherein

the external terminal is an I/O terminal for data input to and data output from the memory cell array.

11. (Withdrawn) The memory circuit according to claim 6, wherein

depending on the data latched by the redundant latch circuit, a pre-charge path is closed which leads to the pre-charge circuit corresponding to the failed point.

12. (New) A memory circuit comprising:

a regular memory cell array having a plurality of redundant replacement units;

a plurality of input/output circuits each of which corresponds to the plurality of redundant replacement units;

a redundant memory cell array with which the redundant replacement unit having a failed portion in the regular memory cell array is replaced;

a redundant replacement memory for storing data on the redundant replacement unit having the failed portion in the regular memory cell array; and

a pre-charge circuit having pre-charge switches for redundant replacement units and the redundant memory cell array respectively, wherein

depending on the data stored in the redundant replacement memory, the redundant replacement unit having the failed portion in the regular memory cell array is or is not replaced with the redundant memory cell array,

in case where a failed portion does not exist in the regular memory cell array, the pre-charge switches of the plurality of redundant replacement units are enabled, and the pre-charge switch of the redundant memory cell array is not enabled, and

in case where a failed portion exists in the regular memory cell array, the pre-charge switch of the redundant replacement unit having a failed portion is disabled and the pre-charge switches of the remaining redundant replacement units and the redundant memory cell array are enabled.